**DVP test**

Revision history

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| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-09-14 | Initial | HuiboZhong |
| 0.2 |  |  |  |
|  |  |  |  |

# 1. IP overview

## DVP Design for Test guidelines

|  |  |
| --- | --- |
| DVP Pad input | Signal name |
| QE0\_0\_PAD | QE0\_0\_PAD |
| QE0\_1\_PAD | QE0\_1\_PAD |
| QE0\_2\_PAD | QE0\_2\_PAD |
| QE0\_3\_PAD | QE0\_3\_PAD |
| QE0\_4\_PAD | QE0\_4\_PAD |
| QE0\_5\_PAD | QE0\_5\_PAD |
| QE0\_6\_PAD | QE0\_6\_PAD |
| QE0\_7\_PAD | QE0\_7\_PAD |
| QE1\_0\_PAD | QE1\_0\_PAD |
| QE1\_1\_PAD | QE1\_1\_PAD |
| QE1\_2\_PAD | QE1\_2\_PAD |
| QE1\_3\_PAD | QE1\_3\_PAD |
| QE1\_4\_PAD | QE1\_4\_PAD |
| QE1\_5\_PAD | QE1\_5\_PAD |
| QE1\_6\_PAD | QE1\_6\_PAD |
| QE1\_7\_PAD | QE1\_7\_PAD |
| PCLK0\_PAD | PCLK0\_PAD |
| DE0\_PAD | DE0\_PAD |
| VSYNC0\_PAD | VSYNC0\_PAD |
| HSYNC0\_PAD | HSYNC0\_PAD |
| PCLK1\_PAD | PCLK1\_PAD |
| DE1\_PAD | DE1\_PAD |
| VSYNC1\_PAD | VSYNC1\_PAD |
| HSYNC1\_PAD | HSYNC1\_PAD |

SPI PAD

|  |  |
| --- | --- |
| PAD name | Signal name |
| SPI\_MS3\_DI | SPI\_DBG\_DI |
| SPI\_MS3\_DO | SPI\_DBG\_DO |
| SPI\_MS3\_SCLK | SPI\_DBG\_SCLK |
| SPI\_MS3\_CS0N | SPI\_DBG\_CSN |

# 2. ATE test

## 2.1 DVP input test

Step :

1. Set pin share setting by spi
2. Set dvp registers (delay phase setting)
3. Enable video\_if by spi write video\_if register
4. Inject dvp signal through dvp related pad.
5. Read video\_if status by spi to check if dvp input is valid.
6. Reset video\_if, change dvp phase,
7. Release reset, read video\_if status by spi to check if dvp input is valid.

## 2.1 DVP output test

Step :

1. Pin share setting by spi,
2. Set dvp registers (delay phase setting)
3. Enable pixel pll by spi write register
4. Check PCLK0\_PAD if the clock is valid.
5. Change clock phase , repeat step4